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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MCLEAN MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/667,050	BOGIN ET AL.	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 27 December 2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 8,9,12-15,17,19-21 and 30-32 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 8-9, 12-15, 17, 19-21 and 30-32 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 22, 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8-9, 12-14 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Dickey (USPN: 6,625,673).

Regarding claim 8, Jeddeloh discloses populating entries within a table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory (the conversion table translates addresses from a graphics controller to a physical address and thus it is evident that the table is populated with the required information/data/addresses to effectuate such functionality); using a conversion table (Figure 2, Reference 202) to translate a first address (untranslated address from the graphics controller) from a graphics controller (Figure 2, Reference 140) to a second address (translated first address) to a memory (C 6, L 17-

24, L 36-50); and using the conversion table to translate a third address (untranslated address from the bus controller) from a bus controller (Figure 2, Reference 130) to a fourth address (translated third address) to the memory (C 6, L 17-24, L 36-50). Jeddeloh does not disclose the physical address having a greater number of bits than the virtual address to enable access to the main memory above a physical address range limit imposed by a register/bus width, a second address having a greater number of bits than the first address and the fourth address having a greater number of bits than the third address. However, Dickey teaches mapping a first address to a second address, wherein the second address has a greater number of bits than the first address to enable access to the main memory above a physical address range limit imposed by a register/bus width (C 2, L 17-31, C 3, L 53-67). This feature taught by Dickey provides an efficient way for providing larger memory space (C 2, L 41-45) and hence, it would have been obvious to one of ordinary skill in the art to incorporate Dickey's teachings with the system taught by Jeddeloh for the desirable purpose of efficiency and flexibility.

Regarding claim 9, the system taught by Jeddeloh and Dickey discloses the conversion able to translate the third address including a translation lookaside buffer (Jeddeloh – C 6, L 25-35).

Regarding claims 12-14, Jeddeloh and Dickey disclose the conversion table including comparing a first portion (virtual/linear address excluding the offset) of the third address (virtual/linear address) with entries in a first table and if the first portion matches a particular one of the entries in the first table, combining a value (physical page number/address) associated with the

particular one with a second portion (offset) of the third address to form the fourth address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that the virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3), and if the first portion does not match any of the entries in the first table, referring to a second table (comprehensive table) to translate the third address (Jeddeloh; C 6, L 30-34; C 7, L 12-15), wherein the comparing includes comparing the first portion of the third address with entries in the first table (GART table) in an input-output controller (Figure 2, Reference 102) and wherein the referring to the second table includes referring to the second table (comprehensive table) in main memory (system memory)(C 6, L 30-34; C 7, L 12-15).

Regarding claims 30-31, Jeddeloh discloses an address translator including a translation lookaside buffer (Figure 2, comprised of References, 124 and 202, [the translation table stored in GART]) and having a first interface to couple to a memory controller (signal line(s) within Reference 124 coupled to Reference 122), a second interface to couple to a graphics controller (signal line(s) within Reference 124 coupled to Reference 140), a third interface to couple to a bus controller (signal line(s) within Reference 124 coupled to Reference 130) and a table of entries, each entry having a first portion and a second portion (Figure 2, Reference 202; table stored within GART); a translation control circuit coupled to the address translator to program

the entries in the address translator to map virtual addresses of a memory range allocated to the graphics controller to physical addresses within the main memory(the address translator comprises interfaces and a table, wherein neither of these elements have logic to control the operation of the address translator and thus it is evident that logic is coupled to the address translator for controlling its operations such as storing/programming addresses/entries in the table); wherein the address translator is to translate an address on the third interface into a first address on the first interface and to translate an address on the second interface into a second address on the first interface (C 6, L 36-50 - Jeddeloh discloses that addresses are received from any of the elements coupled to Reference 124 in Figure 2, and are translated using the table in the GART as long as the address falls within a reserved range of addresses). Jeddeloh does not disclose the address translator translating an address on the third interface into a first address on the first interface having a greater number of bits than the address on the third interface nor translating an address on the second interface into a second address on the first interface having a greater number of bits than the address on the second interface or the physical addresses having a greater number of bits than the virtual addresses. However, Dickey teaches the concept of mapping/translating an initial address (I/O address) into a first address (larger system memory address), wherein the first address has a greater number of bits than the initial address to enable access to the main memory above a physical address range limit imposed by a register/bus width (C 2, L 17-31, C 3, L 53-67). This feature taught by Dickey provides an efficient way for providing larger memory space (C 2, L 41-45) and hence, it would have been obvious to one of ordinary skill in the art to incorporate Dickey's teachings with the system taught by Jeddeloh for the desirable purpose of efficiency and flexibility.

Regarding claim 32, Jeddeloh and Dickey disclose the address translator comprising a graphics translation lookaside buffer (Figure 2, Reference 202 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]).

4. Claims 15, 17 and 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeddeloh (USPN: 6,477,623) in view of Dickey (USPN: 6,625,673) and Bryg et al. (USPN: 5,060,137).

Regarding claim 15, Jeddeloh discloses an apparatus comprising a translation lookaside buffer (Figure 2, Reference 202 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]); control logic coupled to the translation lookaside buffer (hardware/software responsible for controlling Reference 202), wherein the control logic populates entries within a table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory (the conversion table translates addresses from a graphics controller to a physical address and thus it is evident that the table is populated with the required information/data/addresses to effectuate such functionality), wherein the control logic is to compare a first portion (virtual/linear address excluding the offset) of an initial address from a bus controller (virtual/linear address from bus controller, Reference 130 in Figure 2) with entries in the translation lookaside buffer and if a first matching entry is found, to combine a first value (physical page number/address) associated with the matching entry with a second portion (offset) of the initial address to form a first translated address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that

the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that a virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3); wherein the control logic is further to access a table (comprehensive table) in memory if the matching entry is not found (C 6, L 30-34, C 7, L 12-15), find a second value (physical page number/address) in the table associated with the first portion, combine the second value with the second portion to form a second translated address (a physical address is formed by combining the physical page number with the offset of the initial virtual/linear address). Jeddeloh does not disclose the first translated address having a greater number of bits than the virtual address to enable access to the main memory above a physical address range limit imposed by a register/bus width, the second translated address having a greater number of bits than the initial address or the physical addresses having a greater number of bits than the virtual addresses, an input register and an output register coupled to the TLB and to the control logic, wherein the control logic is to compare a portion of an initial address in the input register with entries in the TLB and holding a first translated address in the output register and holding a second translated address in the output register. However, Dickey teaches mapping a first address into a second address, wherein the second address has greater bits than the first address to enable access to the main memory above a physical address range limit imposed by a register/bus width (C 2, L 17-31, C 3, L 53-67). This feature taught by Dickey provides an efficient way for providing larger memory space (C 2, L 41-45) and hence, it would have been

obvious to one of ordinary skill in the art to incorporate Dickey's teachings with the system taught by Jeddeloh for the desirable purpose of efficiency and flexibility. Additionally, Bryg teaches a TLB (Figure 2) coupled to an input register (Figure 2, Reference 1; C 3, L 29-30) and an output register (Figure 3, Reference 31; C 3, L 65-67) and control logic (software or hardware logic for controlling the operation of the TLB), wherein the control logic is to compare an initial address in the input register with the entries in the TLB (C 3, L 43-61) and wherein a translated address is held in the output register (Figure, 2; PHYSICAL ADDRESS TO CACHE; C 3, L 65-67; Figure 3, PHYSICAL ADDRESS). It is well known in the art to store data/addresses in a register for the purpose of reducing jitter and glitches from the signals thereby providing accurate and stable data outputs. Jeddeloh addresses are not disclosed as stored in registers and thus are vulnerable to the effects of glitches and jitter. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Dickey and Bryg with the teachings of Jeddeloh for the desirable purpose of expanding the address capability of a system by allowing the system to access a larger amount of physical memory and thereby improving the performance of the system and for the desirable purpose of providing stability and accuracy.

Regarding claim 17, Jeddeloh, Dickey and Bryg disclose the control logic including logic for first and second control flows, wherein the second control flow is to translate an initial graphics controller address and does not access the table (Jeddeloh – C 7, L 9-12; the control logic responsible for translating an address using the GART, when a GART hit occurs) and wherein the first control flow is to translate an initial bus controller address and accesses the table

(Jeddeloh – C 7, L 12- 15; the control logic responsible for translating an address using the comprehensive table in system memory – when a GART miss occurs).

Regarding claim 19, Jeddeloh discloses a processor (Figure 1, Reference 116); a memory (Figure 1, Reference 104); a graphics controller (Figure 1, Reference 140); a bus controller (Figure 1, Reference 118); an input-output controller coupled to the processor, memory, graphics controller and bus controller (Figure 2, input-output controller is comprised of References 122, 124, 130, 202, 126, and 204), the input-output controller including a translation lookaside buffer (TLB)(Figure 2, Reference 202 -Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses [C 6, L 28-30]); control logic coupled to the translation lookaside buffer (hardware/software responsible for controlling Reference 202), wherein the control logic populates the entries within a table to map virtual addresses of a memory range allocated to a graphics controller to physical addresses within main memory (the conversion table translates addresses from a graphics controller to a physical address and thus it is evident that the table is populated with the required information/data/addresses to effectuate such functionality); wherein the control logic is to compare a first portion (virtual/linear address excluding the offset) of a first initial address (virtual/linear address) from the bus controller (via Reference 130) (C 6, L 36-50) with entries in the translation lookaside buffer and if a first matching entry is found, combining a first value (physical page number/address) associated with the first matching entry with a second portion (offset) of the first initial address to form a first translated address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses

(C 6, L 28-30) and thus TLBs function such that a virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3); and wherein the control logic is further to compare a first portion of a second initial address from the graphics controller (Figure 2, Reference 140; C 6, L 36-50) with the entries in the translation lookaside buffer and if a second matching entry is found, to combine a second value (physical page/frame number) associated with the second matching entry with a second portion of the second initial address (offset portion) to form a second translated address (physical address) (Figure 3, References 310, 312; C 7, L 9-18 - Jeddeloh discloses that the GART table is a TLB for addresses in the reserved range of graphics addresses (C 6, L 28-30) and thus TLBs function such that the virtual/linear address, [excluding the offset], is compared to the addresses in the TLB and when a match is found, a physical address is formed by combining the physical page number [translated address] with the offset of the virtual/linear address and thus it is evident that these steps are performed when performing steps 310 and 312 in Figure 3. These same steps are performed for each address provided thereto from any of the elements coupled to Reference 124 in Figure 2 for translation). Jeddeloh does not disclose the first translated address having a greater number of bits than the virtual address to enable access to the main memory above a physical address range limit imposed by a register/bus width, the second translated address having a greater number of bits than the initial address or the physical addresses having a greater number of bits than the virtual addresses, an input register and an output register coupled to the TLB and to the control logic, wherein the control logic is to compare a portion of an initial

address in the input register with entries in the TLB and holding a first translated address in the output register and holding a second translated address in the output register. However, Dickey teaches mapping a first address into a second address, wherein the second address has greater bits than the first address to enable access to the main memory above a physical address range limit imposed by a register/bus width (C 2, L 17-31, C 3, L 53-67). This feature taught by Dickey provides an efficient way for providing larger memory space (C 2, L 41-45) and hence, it would have been obvious to one of ordinary skill in the art to incorporate Dickey's teachings with the system taught by Jeddeloh for the desirable purpose of efficiency and flexibility. Additionally, Bryg teaches a TLB (Figure 2) coupled to an input register (Figure 2, Reference 1; C 3, L 29-30) and an output register (Figure 3, Reference 31; C 3, L 65-67) and control logic (software or hardware logic for controlling the operation of the TLB), wherein the control logic is to compare an initial address in the input register with the entries in the TLB (C 3, L 43-61) and wherein a translated address is held in the output register (Figure, 2; PHYSICAL ADDRESS TO CACHE; C 3, L 65-67; Figure 3, PHYSICAL ADDRESS). It is well known in the art to store data/addresses in a register for the purpose of reducing jitter and glitches from the signals thereby providing accurate and stable data outputs. Jeddeloh addresses are not disclosed as stored in registers and thus are vulnerable to the effects of glitches and jitter. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the teachings of Dickey and Bryg with the teachings of Jeddeloh for the desirable purpose of expanding the address capability of a system by allowing the system to access a larger amount of physical memory and thereby improving the performance of the system and for the desirable purpose of providing stability and accuracy.

Regarding claim 20, Jeddeloh, Dickey and Bryg disclose the control logic is further configured to access a table (comprehensive table) in memory if the first matching entry is not found (comprehensive table) to translate the third address (Jeddeloh - C 6, L 30-34; C 7, L 12-15), find a third value (physical page/frame number) in the table associated with the first portion of the first initial address, combine the third value with the second portion of the first initial address to form a third translated address (Jeddeloh - Figure 3, References 310, 312 - the third value and the offset of the first initial address are combined to perform a memory operation and are thus combined to form a physical address) and hold the third translated address in the output register (Bryg).

Regarding claim 21, Jeddeloh, Dickey and Bryg disclose the control logic including logic for first and second control flows, wherein the second control flow is to translate an initial graphics controller address and does not access the table (Jeddeloh – C 7, L 9-12; the control logic responsible for translating an address using the GART, when a GART hit occurs) and wherein the first control flow is to translate an initial bus controller address and accesses the table (Jeddeloh – C 7, L 12- 15; the control logic responsible for translating an address using the comprehensive table in system memory – when a GART miss occurs).

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 571-272-4194. The examiner can normally be reached on Mon, Wed, Thurs (10-4), Tues (9:45 - 6:15).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KIMBERLY MCLEAN-MAYO
PRIMARY EXAMINER

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KNM

January 5, 2007